



**A Novel Architecture for Signal & Power Optimization for AI/HPC**: The demand for extremely high data bandwidth (~terabyte-per-second) and extensive input/output connectivity has grown significantly for artificial intelligence (AI) and high-performance computing (HPC) applications. To meet it, advanced packaging techniques have become essential and silicon interposers, known for their high-density interconnects, have been widely adopted. But they bring challenges related to the complexity of their redistribution layers (RDLs) and the inherent limitations of through-silicon vias (TSVs). Adding additional RDL layers can improve power delivery network performance, but the increased thickness can induce wafer warpage due to stress accumulation. Similarly, although high-aspect-ratio TSVs improve integration density, they introduce issues such as potential void-free filling, stress management problems and increased fabrication complexity.

To overcome these challenges, at ECTC a HANA Micron-led team will propose a heterogeneous integrated chip (HIC™) for 2.xD packaging for wide I/O applications. It uses bridge dies and copper posts instead of a conventional silicon interposer. The design integrates signal and power routing within the bridge die structure and copper posts, eliminating the need for a dedicated frontside RDL and C4 bumps. As a result, routing path lengths are reduced, parasitic RC delays are lowered, and power delivery network formation is simplified, improving both signal and power integrity. The proposed design supports up to 6.4 Gbps per lane in a staggered configuration, suitable for HBM3 high-speed connectivity, and the researchers will highlight its potential as a scalable, cost-effective solution for next-generation high-speed packaging applications.

**The images above show**:

* Top left: A mechanical prototype of the heterogeneously integrated chip on a 70 mm × 70 mm package substrate.
* Top right: A conceptual illustration with the bridge dies and copper posts highlighted in yellow.
* Bottom: Eye diagrams of the silicon interposer channel in the (a) split and (b) staggered configurations, and also of the RDL bridge die channel in the (c) split and (d) staggered configurations.

**(IP session #38, “*Signal and Power Integrity Optimization Using Novel Bridge Die and Copper Post Interconnect Design in 2.xD Packaging for Wide I/O Applications*,” Y. Na et al, HANA Micron Inc./ Myongji University/ Swevenz Inc.)**